

A reconfigurable test bed for communication EW systems

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Abstract:

Testing and validating Electronic Warfare (EW) receiver systems is a challenging task and requires customized instrumentation setup. An FPGA based reconfigurable core is developed which is capable of generating any complex EW signal scenario, which is mainly useful in communication Electronic Support Measures (ESM) receiver testing and validation. The developed core can be used for either injection mode testing to evaluate receiver subsystem, or as FPGA on chip test signal generator for module level testing. The core provides various options in form of compile time option and run time options, by which user can generate multisignal scenario. The pipelined CORDIC algorithm based universal modulator is the critical block of the total core. The developed core is verified on NSS-FD2-01 hardware platform running with Virtex-6 FPGA. The maximum clocks speeds observed are 215 MHz, while occupying only 15% of Virtex-6 LX240T for generating three types of modulated signals including two FHSS with 2000 hops/sec and one CW signal.

Key Words: EW test bed, test signal generator (TSG), Automated test equipment (ATE), radiation mode, injection mode, FH simulator

I INTRODUCTION

Testing and validating against a given set of specifications under practical conditions is the most crucial part in development of EW systems. The very known methods of testing include injection mode and radiation mode. In injection mode testing the signal is injected into the system under test (SUT), where as in radiation mode testing the signal is radiated and the SUT is tested including the antenna.

In radiation mode testing the system is tested as a whole and it leaves less scope for individual system level debugging. Hence such kind of testing becomes useful only in the final phase of system evaluation. In injection mode testing the signal is injected into the system with appropriate characteristics. This method avoids the need of antenna and LNA front end for testing the RF modules and/or IF subsystems and down the chain subsequent digital modules in the EW receiver. However this method also becomes useful for sub system level testing only and is limited by the type of signals that can be generated and injected.

The most common technique is to use signal generators for injecting the signal into the ADC of the system. The present day signal generators[2][3] are capable of generating all modulation signals with programmable parameters. However they are capable of generating only one or two signal scenarios.

At present the market available simulators provide simulation models for communication systems, but they are not useful for generating test signals for verifying hardware implemented algorithms.

The paper[4] describes the ultra wide band communication system simulation aspects. The simulator described in [5] proposes mainly the channel simulation aspects and wave propagation issues. This presents architecture for interacting with real hardware, so that a transmitter and receiver with in between simulated propagation conditions can be verified. The HF communication simulator given in [6] performs the jamming signal simulation at the RF level. The simulation of complete communication system is described in [7] for tactical communications. Most of the work presented in past, either explain full simulation studies or modeling channel or multipath conditions.

In comparison with the previous work, the presented work is capable of generating multiple communication signals along with channel models, which is capable of generating the signals either at base band or in pass band. This is the most suitable simulator for validating the communication ESM systems. The conventional base band simulation [6] cannot bring out all practical aspects which are involved in true RF/IF level testing. Hence the proposed core offers both the output types. As the current EW systems are powered by the DSP algorithms and high speed digital circuits, there is a need for module level testing and validation.

II High level architecture

The diagram given below shows the high level architecture for the developed FPGA core

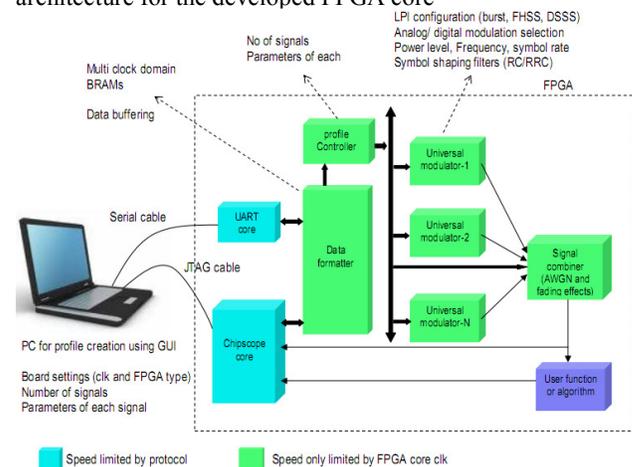


Figure 1. High level architecture

The developed FPGA based reconfiguration test bed can be used either as a FPGA firmware to directly embed in the user FPGA of the SUT, or it can be used as a separate test bed by installing on COTS FPGA hardware. While the second mode of usage gives all benefits of injection mode testing, the first mode allows module level testing without demanding for additional hardware.

The developed reconfigurable communication signal generator can generate LPI and Spread spectrum signals such as FHSS, DSSS and Burst. The DSSS signal can be with different types of PN code generators (Gold, ML and Kasami). The supported analog and digital modulations are AM-DSBSC, AM-DSBFC, AM-SSB, FM, OOK, BPSK, BFSK, M-PSK, 16-QAM and 64-QAM. The pipelined CORDIC algorithm along with modulator blocks is used as universal modulator to generate various modulation types of signals. The core consists of options in which some of them are to be selected at compile time, and rest of them can be selected dynamically. The user will select the required compile time options, which are usually the hardware parameters of sub system under test, such as IF band width, center frequency, ADC sampling rate and builds the FPGA netlist for test bed core. Once the test bed core is combined with user application then bit file can be created. The bit file when it is programmed to FPGA, then the test bed core shall be controlled through PC for changing the dynamic parameters.

The Core connects through UART to the GUI that is running in PC. UART is selected as it takes negligible area on FPGA and any COTS FPGA board shall readily the connector for UART communication.

The below two figures show important GUI controls by which dynamically the user can change the signal scenario.

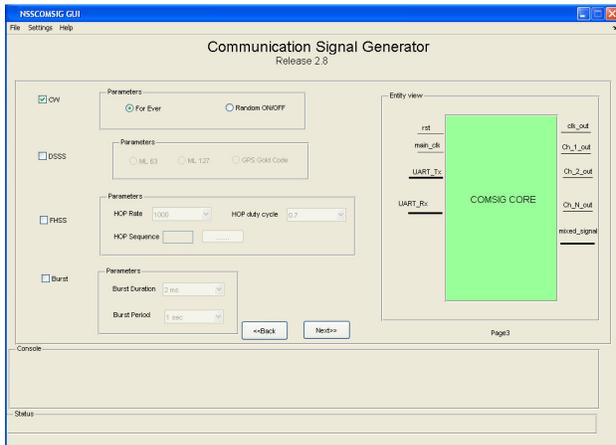


Figure 2. GUI - Spread spectrum and LPI selection

The signal scenario is described through The top level profile which selects multiple signals with required parameters along with noise and multipath parameters.

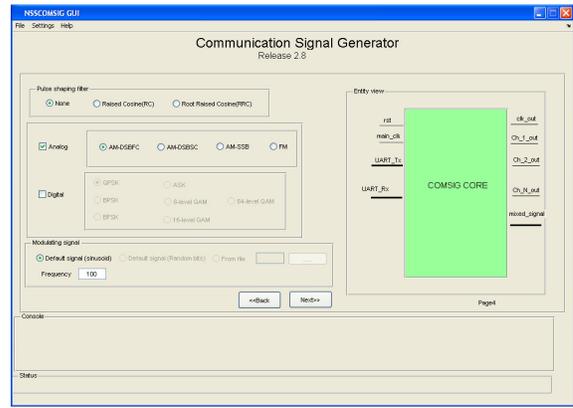


Figure 3. Modulation options

The UART core output is connected to dual port BRAM by which the commands are set to all other modules. The true DPRAM shall ensure that the parameter setting is in CORDIC module clock domain without any linking to clocks or baudrates associated to UART.

The profile generator ensures the number of signals currently being active as per the settings made on PC GUI. The universal modulator logic is realized as shown in below figure.

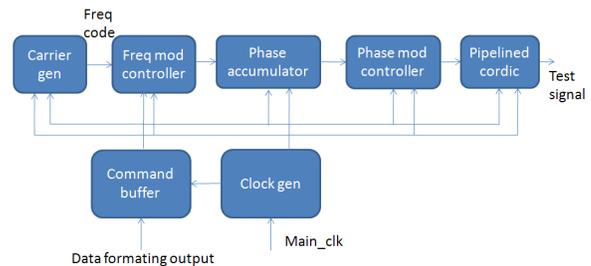


Figure 4. Universal modulator

The carrier gen block produces the frequency code based on the FHSS or CW settings. The frequency mod controller block performs the necessary shift on frequency based on the modulating signal. The BFSK and other modulation types in which frequency gets affected are implemented in this block. The modulating signal is either randomly generated with in FPGA core or taken from file at the time of generating core. In PC with ASCII values can be given as modulating signal.

The phase accumulator generates the digital phase based on the frequency word. The phase mod controller alters the phase based on the modulating signal. The digital phase wraps on all 1s and becomes zeros corresponding to 2π radians. The pipelined CORDIC is implemented to generate SIN and COS samples for given phase input.

III. Pipelined CORDIC

CORDIC algorithm is useful for computing the COS and SIN outputs corresponding to given angle θ . The paper [8] describes the pipelined CORDIC implementation and architecture for implementing the low latency outputs.

$$\begin{aligned} x' &= x \cos \phi - y \sin \phi \\ y' &= y \cos \phi + x \sin \phi \end{aligned} \quad (1)$$

The CORDIC algorithm rotates the phasor by angles which are tan inverse of 2^{-i} , for integers of i . By these techniques the algorithm implements COS and SIN functions without any multiplication. As the theory of CORDIC is well discussed in literature [8][9] it is not discussed here. The pipelined CORDIC architecture is implemented as per the below given RTL. As the logic need to be generated as per the options chosen in GUI panel, VHDL Generic based RTL code is developed.

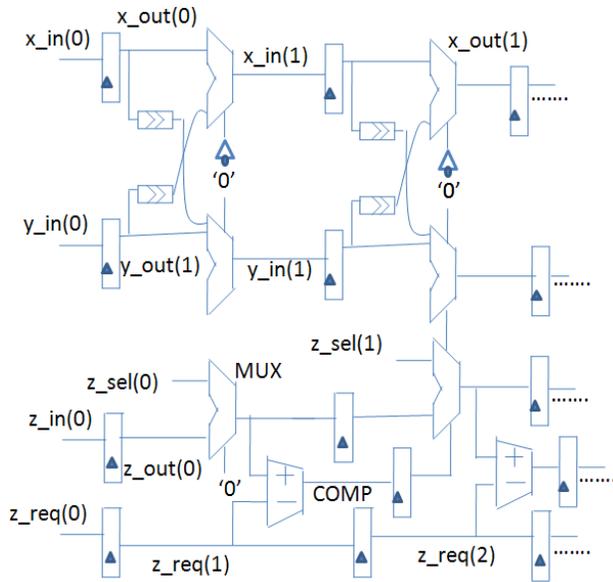


Figure 5. Pipelined CORDIC

IV. Results

The core is simulated with Modelsim and the results are verified correct for both functional simulation and timing simulation. The below figure shows the screen shot of results for various modulation types.

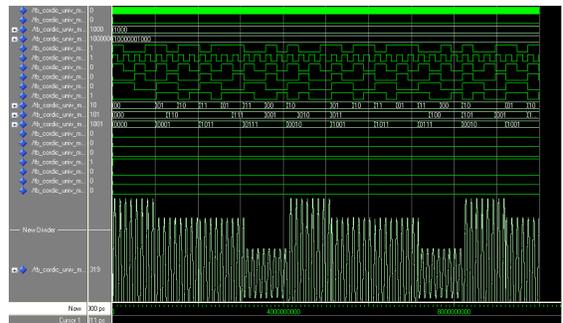
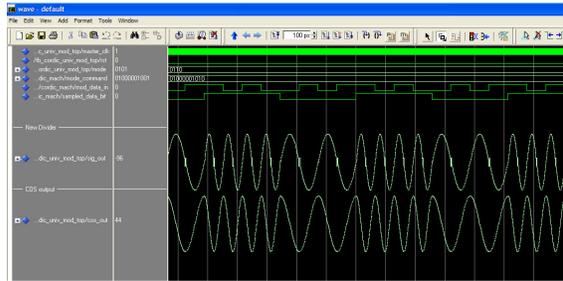
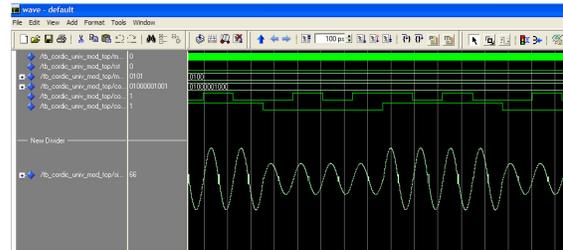
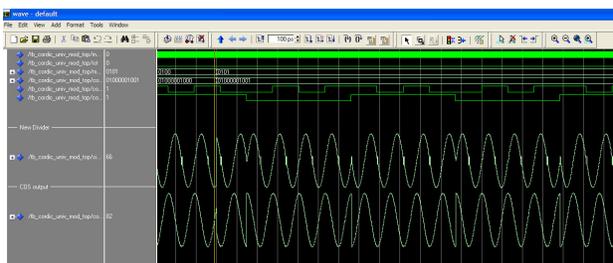


Figure 6. Results for BPSK, ASK, BFSK and 16 QAM

V. CONCLUSION

A reconfigurable FPGA based core is developed for generating multi signal scenario with all practical effects such as multipath and noise. The typical communication ESM system validation requirements are considered while developing the core. The core is capable for on chip testing on FPGA and also as injection mode test signal generator when it is ported FPGA-DAC hardware.

The developed core is verified on NSS-FD2-01 hardware platform running with Virtex-6 FPGA. The maximum clocks speeds observed are 215 MHz, while occupying only 15% of Virtex-6 LX240T for generating three types of modulated signals including two FHSS with 2000 hops/sec and one CW signal.

The core is successfully used for testing EW algorithms at NSS labs and being upgraded to include OFDM and STBC type of schemes

Note: Additional information on the IP benchmarks for Various FPGAs and performance analysis are available on request.

REFERENCES

- [1] Mark Kahrs and Christopher Zimmer, "Digital Signal Processing in a Real-Time Propagation Simulator," IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 55, NO. 1, FEBRUARY 2006
- [2] R&S SMU200A vector signal generator
- [3] Agilent technologies E4438C ESG Vector Signal Generator
- [4] Sylvain Chaillon, Didier Helal, Chiara Cattaneo, "Timed simulator for UWB communication systems," 2002 IEEE conference on Ultra Wideband Systems and Technologies
- [5] Mark Kahrs and Christopher Zimmer, "Digital Signal Processing in a Real-Time Propagation Simulator," IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL.55, NO.1, FEBRUARY2006
- [6] Birch, S.W and Davies, N.C., "An advanced HF communications simulator, HF Radio Systems and Techniques," Seventh International Conference on (Conf. Publ. No. 441) 1997
- [7] Antkiewicz, R.Manikowski, A.;Najgebauer, A.;Nowicki, T." *A computer simulator of a tactical communication system,*" IEEE Military Communications Conference. Proceedings. MILCOM 98 (Cat. No.98CH36201)
- [8] Elisardo Antelo and Julio Villalba, "Low Latency Pipelined Circular CORDIC," Proceedings of the 17th IEEE Symposium on Computer Arithmetic (ARITH'05)
- [9] Chen Shijie and Houjun wang, "A study of signal generation based on CORDIC algorithm". IEEE conference 2005

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S. Krishna Prasad received B.Tech degree in year 2009 in Electronics and Communications Engineering from JNTU Hyderabad, INDIA. He completed his training at NSS Communication Labs for Electronic Warfare system design. Currently He is working for development of ESM systems on FPGA platforms.